PVP 12

Code: **ECMC2T6C**

I M.Tech-II Semester–Regular/Supplementary Examinations – July 2017

DSP PROCESSORS AND ARCHITECTURES
(MICROWAVE & COMMUNICATION ENGINEERING)

Duration: 3 hours Max Marks: 70

Answer any FIVE questions. All questions carry equal marks

1. a) What is the advantage of multirate processing and explain about decimation and interpolation with example applications. 7 M

   b) Draw the suitable block diagram of digital signal processing system and explain briefly. 7 M

2. a) Explain the fixed-point format and floating-point format for signals and coefficients in DSP systems. 7 M

   b) Explain D/A conversion errors. 7 M

3. a) What are the sources of errors in implementation? Briefly explain each of them and technique to minimize. 7 M

   b) Discuss in detail about the features required for external interfacing of DSP device. 7 M

4. a) Describe Interrupts and Stacks. 7 M

b) Explain pipeline operation of TMS320C54XX processor with example. 7 M

5. a) Describe Host Port Interface and explain its signals. 7 M

b) Explain the operation of serial I/O ports and hardware timer of TMS320C54XX on chip peripherals. 7 M

6. a) Draw the diagram of a fixed point data path and explain. 7 M

b) What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly-phase sub filter. 7 M

7. a) Discuss in detail about the FFT algorithm for DFT computation with neat diagrams and briefly explain about butterfly computation. 7 M

b) Explain computation of the signal spectrum. 7 M

8. a) Explain how DMA method of data transfer help in increasing the processing speed of a DSP processor. 7 M

b) Explain the CODEC-DSP interface with an example. 7 M